

App. Ser. No. 09/740,174
Atty. Dkt. No. MIO 0042 V2

REMARKS

Claims 35-37 and 51-63 are pending in the present application. Withdrawn claims 38 and 42-50 have been cancelled. Claims 35 and 63 have been amended.

The Examiner rejected claims 35-37 and 51-63 under 35 U.S.C. §102(b) as being anticipated by Canaris et al. According to M.P.E.P. § 706.02, in order to be anticipating under § 102, the reference must teach every aspect of the claimed invention. Regarding amended independent claims 35 and 63, the Examiner has failed to show that Canaris teaches each and every aspect of the claimed invention.

Regarding amended independent claims 35 and 63, the Examiner has failed to show that Canaris teaches that "the first source is coupled to the first voltage input through a parasitic resistance of the well." Instead, as is shown in Figs. 4A and 4B, Canaris only teaches that the source 22 is directly coupled to ground Vss. Canaris states that "the source is coupled to Vss" (Col. 1, line 27; Col. 3, lines 28-37). Additionally, Canaris states that "a P+ guard 40 is tied to ground and surrounding the N-channel transistors" (Col. 3, lines 34-37).

In the Office Action mailed August 12, 2003, the Examiner stated that "the first source 22 is coupled to the first voltage input through a parasitic resistance R_w , R'_w , $R's$, R_s of the well." However, the Examiner is mistaken. Figs. 4A and 4B show that the source 22 is coupled to the voltage input Vss **directly**. Thus, the source 22 **cannot be** coupled to Vss through a parasitic resistance of the well. Nowhere does Canaris suggest that the source 22 is coupled to the voltage input through the parasitic resistances R_w , R'_w , $R's$, or R_s .

Additionally, regarding independent claims 35 and 63, Canaris does not teach "forming a second contact in the well in spaced relation to the first type transistor; coupling the first contact to a first voltage input; and coupling the second contact to the first source" as claimed. Instead, Canaris teaches coupling Vss to the source 22 and to a **guard ring** 40 that surrounds the transistor in the p-well 18 (Col. 3, lines 34-37 and lines 55-64). The guard ring is shown in Figs. 3 and 4A.

Thus, the guard ring 40 is not a first and second contact as the Examiner suggests. Instead, guard ring 40 is a circular area around the transistor. Vss (ground) is coupled to the guard ring 40 and to the source 22 (Col. 3, lines 34-37). The guard ring is tied to Vss

App. Ser. No. 09/740,174
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at a single point, and a parallel resistance $R'w$ is formed in addition to the primary resistance of the well Rw because of the connection of the guard ring 40 to Vss (Col. 3, lines 65-68; Col. 4, lines 1-3). Fig. 4B shows the equivalent circuit for the parasitic transistors, and it can be seen that Vss is tied to the guard ring 40 at one point because a single parallel resistance $R'w$ is formed. Fig. 4A shows a connection from the right side of the guard ring 40 to Vss , and a connection from the left side of the guard ring 40 to Vss . However, these connections are schematic illustrations of a single connection to Vss for the circular region 40. Thus, Canaris does not teach coupling the second contact to the first source because there is no second contact.

Claims 36, 37 and 51-62 depend from independent claim 35. Thus, claims 35-37, 51-62, and 63 are patentable over the cited and applied prior art.

App. Ser. No. 09/740,174
Atty. Dkt. No. MIO 0042 V2

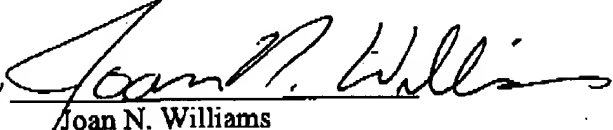
CONCLUSION

Applicants respectfully submit that, in view of the above amendments and remarks, the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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